Modelling of the Basic Parameters for Gaussian doped Symmetric Double Halo Dual Material Gate n-MOSFET

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Abstract: A model for sub threshold surface potential and threshold voltage for a Double halo Dual Material Gate (DHDMG) MOSFET is proposed in this paper. To model the sub threshold surface potential, a pseudo-2D analysis applying Gauss's law along the surface is used. This is also used to find the threshold voltage for Gaussian profile based DHDMG. Two Gaussian pile-up profiles are located at the source and drain ends of a MOSFET. The proposed model is derived on the basis of this and is further applied to find the surface potential using high-k gate dielectric materials. In order to verify the models, a 2D device simulator DESSIS is used and simulation results reveal that the model predicts the value of the sub threshold surface potential and threshold voltage almost accurately for the different devices and pocket parameters along with various bias voltages.
Keywords: Gaussian doping; sub threshold surface potential; threshold voltage; double halo; gauss's law.

1 INTRODUCTION

Higher speed and an improved performance over the traditional MOSFETs are obtained by considerably reducing the dimension of MOSFETs. Nowadays, for large scale integration the power consumption of modern VLSI circuits has become very significant. An effective way for reducing this potential is to scale down the power supply voltage.

Present day MOSFETs are either vertical non-uniformly doped or lateral non-uniformly doped. To model the surface potential and threshold voltage accurately the most important factor is to model its non-uniform doping profile.

Considering Gaussian profile based pockets, a quasi-Fermi potential based analytical sub threshold surface potential and threshold voltage model for sub 40 nm DHDMG MOSFET has been derived in this paper. An average doping profile expression is used to find the expression of the characteristic parameters. It is known from the

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simulation results that the value of the sub threshold surface potential and the threshold voltage is predicted accurately for different device and doping profile parameters along with various bias voltages. The validity of our model for analog circuits in 30 nm sub threshold regime is, hence proved.

2 MODEL DESCRIPTION

Many implantation and diffusion steps in the fabrication process are required. For this reason, Gaussian doping profile has replaced other profiles for practical MOSFETs. Better characteristics for DHDMG MOSFETs are thus obtained by modeling of characteristic parameters using a Gaussian doping profile as in Fig. 1.

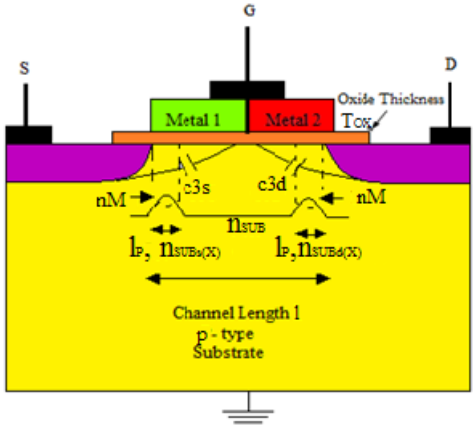

Fig. 1. Structure of n-channel gaussian doped dhdmg mosfets.

Gaussian profiles at the source and drain ends are considered as in Fig. 1. The doping concentration at the source end is

$$\mathbf{n_{SUB,s}(x) = n_M e^{-\{(x/l_P)\}^2}} \quad (1)$$

The distance along the channel is considered as x. With the reduction of channel length, the lateral doping increases. This is due to the overlap of the pile-up profiles as channel length decreases as in [1] and [2]. n_m and l_P stands for the maximum concentration of the Gaussian profile and the horizontal length of the Gaussian regions.
The drain side doping concentration is

$$\mathbf{n_{SUB,d}(x) = n_M e^{-\{(l-x/l_P)\}^2}} \quad (2)$$

The average doping concentration is

$$n_{AV,GAUSS} = n_{SUB} + \frac{l_P}{l} n_M [\int_0^{\frac{l}{l_P}} e^{-P^2} dp - \int_{\frac{l}{l_P}}^{0} e^{-P^2} dp] \quad (3)$$

Combining Equations (1), (2) and (3),

$$n_{AV,GAUSS} = n_{SUB} + n_{M\{} \frac{sqrt(\pi) erf(\frac{l}{l_P})}{\frac{l}{l_P}}\} \quad (4)$$

A small Gaussian box is considered at distance x along the channel of length Δx as in [3] and [4].The height of the box is so chosen that it covers the entire depletion depth. Here y_D = the depletion depth and w = width of the rectangular box and $\Delta x y_D w$ = volume of the box.

Application of Gauss's law leads to

$$\varepsilon \oint \vec{E}.d\vec{s} = -Q\, n_{AV} y_D \Delta x w$$

Here $\vec{E}$ = electric field striking the faces of the box perpendicularly. $\vec{ds}$ = area of the faces.

If ε_{Si} and ε_{OX} stand for permittivity of Silicon and silicon dioxide respectively, the surface potential is given as in Equation (5)

$$\varepsilon_{Si} \frac{d^2\Psi_S}{dx^2} - \frac{c_{OX}}{y_D}\Psi_S = Q n_{AV,GAUSS} - \frac{c_{OX}}{Y_D} v_{gs} \quad (5)$$

Where, $\frac{\varepsilon_{OX}}{T_{OX}} = c_{OX}$= oxide capacitance per unit gate area.

The variation of the depletion layer depth is shown in Fig. 2:

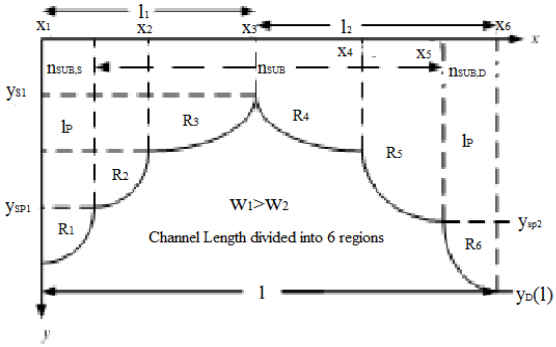

Fig. 2. Variation of depletion layer depth.

Equation (4) can be solved for perfect value of the surface potential as in [3-5]. However $y_D(x)$ need to be modelled for obtaining a perfect solution of the surface potential.

Considering $y_D(x) = (ax + b)^2$, the source and the drain end values are given as in Equations (6) and (7).

$$y_D(0) = x_J + \sqrt{2\varepsilon_{SI(V_1)} / (qn_{AV,GAUSS})} = x_J + x_{RS} \quad (6)$$

and

$$y_D(L) = x_J + \sqrt{2\mathcal{E}_{SI(V_7)}/(qn_{AV,GAUSS})} = x_T + x_{RD} \quad (7)$$

respectively where,

$$v_1 = v_{sb} + v_{BI} + v_{FS}, v_7 = v_{db} + v_{BI} + v_{FD}$$

v_{BI}=substrate built-in potential. v_{sb} and v_{db}=source and drain bias respectively, $n_{AV,GAUSS}$ is the average concentration,

$$x_{RS} = \sqrt{2\mathcal{E}_{SI(V_7)}/(qn_{AV,GAUSS})} \quad (8)$$

and

$$x_{RD} = \sqrt{2\mathcal{E}_{SI(V_7)}/(qn_{AV,GAUSS})} \quad (9)$$

The depth of penetrations of the depletion layers at the source and the drain ends are given in Equations (8) and (9).

The channel is divided into six regions with known values v_1 and v_7. The unknown voltages are obtained by applying the continuity of the electric field at the junction of the different regions. The unknown voltages are obtained by solving Equations (10)-(13).

$$A_{21}v_2 + A_{22}v_3 + A_{23}v_4 + A_{24}v_5 + A_{25}v_6 = a_2 \quad (10)$$

$$A_{31}v_2 + A_{32}v_3 + A_{33}v_4 + A_{34}v_5 + A_{35}v_6 = a_3 \quad (11)$$

$$A_{41}v_2 + A_{42}v_3 + A_{43}v_4 + A_{44}v_5 + A_{45}v_6 = a_4 \quad (12)$$

$$A_{51}v_2 + A_{52}v_3 + A_{53}v_4 + A_{54}v_5 + A_{55}v_6 = a_5 \quad (13)$$

Two fitting parameters $\zeta_S = {}^{v_1}/_{v_{BI}}$ for the source end and $\zeta_D = {}^{v_7}/_{v_{BI}}$ for the drain end are considered for obtaining a best fit surface potential model profile with ISE TCAD. The same model can give accurate expression of surface potential for SHDMG MOSFET[6].

The threshold voltage is the gate voltage v_{gs} at which the minimum subthreshold surface potential

$$\boldsymbol{\psi_{s,MIN} = 2 * \phi_f + v_{sb} + v_{FS}} \quad (14)$$

x_{MIN} corresponding to $\boldsymbol{\psi_{s,MIN}}$ is approximated at the junction between regions 2 and 3 or between regions 3 and 4. An iterative method is used to find the threshold voltage.

3 RESULTS

Using the 2D-device simulator DESSIS of ISE TCAD [7], MOSFET structures are simulated. Metal gate, n-type source and drain contacts and p-type poly-silicon body contact are present in MOSFET structure in Fig. 1. Default values of work functions for the two metals taken are W_1=4.2 eV and W_2=4.1 eV respectively, unless mentioned. The work function of Metal 1 is taken greater than that for Metal 2, in the DHDMG MOSFET. Thus, threshold voltage corresponding to Metal 1(v_{T1}) is greater than that corresponding to Metal 2(v_{T2}). The advantage of improved gate transport efficiency is found here.

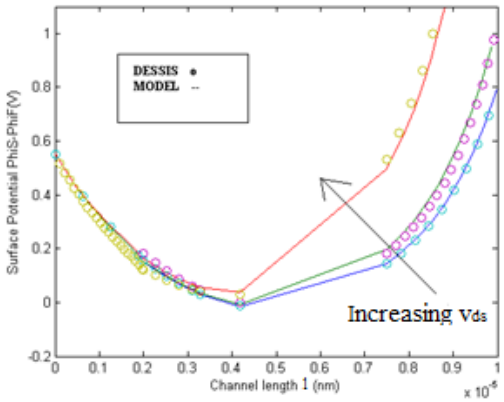

Fig. 3. The plot of surface potential versus channel length of dhdmg mosfet for three different values of the $\boldsymbol{v_{ds}}$=0.25, 0.5 and 0.75 V for l = 100 nm and fixed doping of $\boldsymbol{n_{SUB}}$=6*1017 cm-3, $\boldsymbol{n_{AV,GAUSS}}$=6*1018 cm-3 against the applied voltages $\boldsymbol{v_{gs}}$=0v=$\boldsymbol{v_{gb}}$=$\boldsymbol{v_{sb}}$.

The surface potentials in the channel calculated from our model are illustrated in Fig. 3 for DHDMG MOSFET as in [8], with the channel length l=100 nm at the various drain biases (v_{ds}=0.25, 0.5 and 2 V).

It is seen from Fig. 4 that as the maximum pocket concentration at the two ends increase the average Gaussian doping concentration increases and the peak of the threshold voltage curves increases [8].

Fig. 5 shows that threshold voltage decreases with an increase in the drain bias. The effect becomes more prominent with the decrease of channel length. The lateral electric field becomes less than the transverse electric field as the channel length increases. For shorter channel devices, the lateral electric field is strong at low drain bias. Due to this, the drift current increases when the drain voltage is low. Also when the drain bias goes from low to high the deviation in the threshold voltage is high.

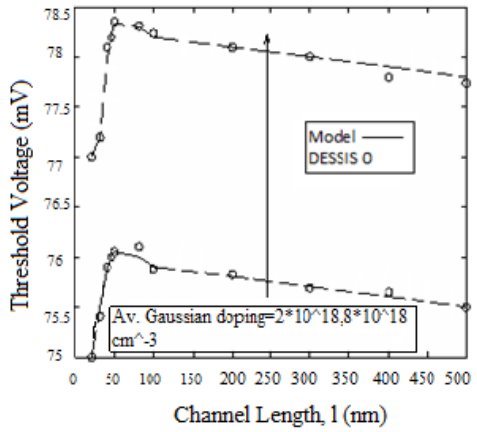

Fig. 4. Plot showing threshold voltage roll-off v/s channel length for $n_{AV,GAUSS}$=2*10^{18} cm^{-3} and 8*10^{18} cm^{-3}.

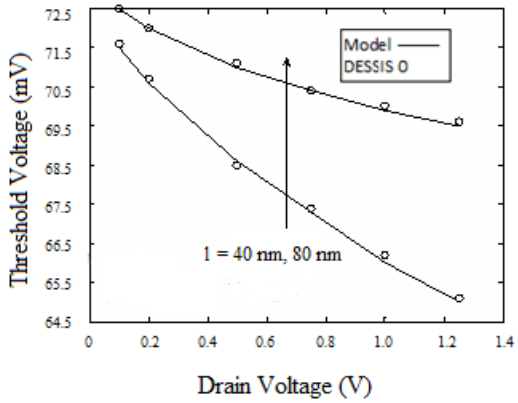

Fig. 5. Plot of threshold voltage v/s drain bias for a gaussian profile based dhdmg n-mosfet for v_{sb}=0 V, v_{ds}=0.5 V for two different channel lengths, l=40 and 80 nm,taking n_{SUB}=5*10^{17} cm^{-3} , $n_{AV,GAUSS}$ =5*10^{18} cm^{-3} , l_P =10 nm.

In semiconductor manufacturing processes, high-k dielectrics are used in place of a silicon dioxide gate dielectric or another dielectric layer of a device. This allows increased gate capacitance without the leakage effects.

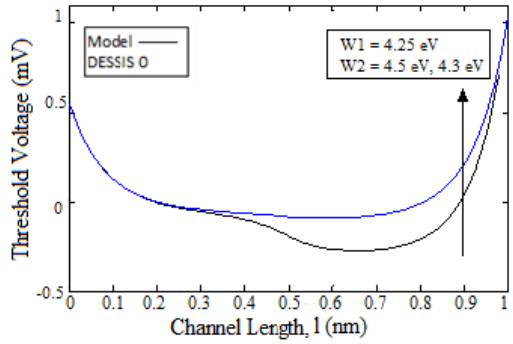

Fig. 6. Plot of surface potential v/s channel length plot for hafnium oxide dielectric obtained by varying work function w2 = 4.5 eV, 4.3 eV and keeping $\boldsymbol{v_{sb}}$= 0 V, $\boldsymbol{v_{gs}}$= 0 V, $\boldsymbol{v_{gb}}$= 0 V, w1 = 4.25 eV and $\boldsymbol{W_s}$= 4.68 eV constant.

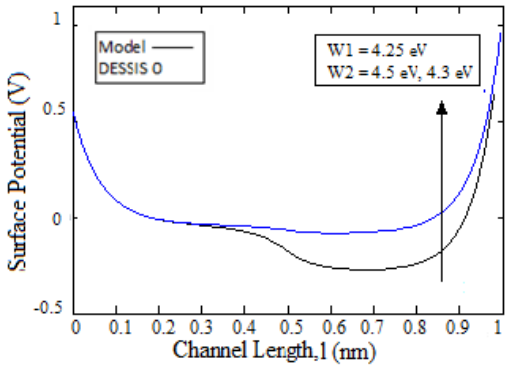

Fig. 7. Plot of surface potential v/s channel length plot for tantalum pentoxide dielectric obtained by varying work function w2 = 4.5 eV, 4.3 eV and keeping$\boldsymbol{v_{sb}}$=0 V, $\boldsymbol{v_{gs}}$= 0 V, $\boldsymbol{v_{gb}}$= 0 V, w1 = 4.25 eV and $\boldsymbol{W_s}$= 4.68 eV constant.

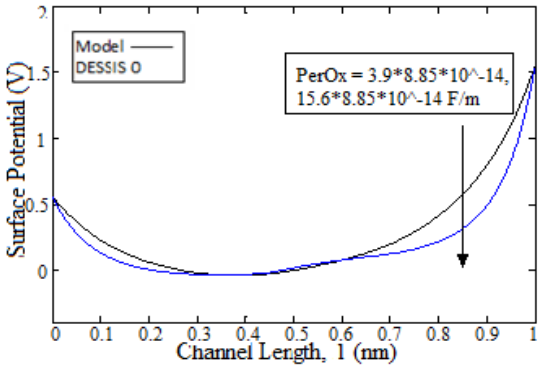

Fig. 8. Plot of surface potential v/s channel length for silicon dioxide and hafnium oxide obtained by varying oxide permittivity using sio2 permittivity = 3.9*8.85*10-14 f/m, hfo2 permittivity = 15.6*8.85*10-14 f/m and keeping $\boldsymbol{v_{sb}}$= 0 V, $\boldsymbol{v_{gs}}$= 0 V, $\boldsymbol{v_{gb}}$= 0 V, w1 = 4.25 eV, w2 = 4.1 eV and ws = 4.68 eV constant.

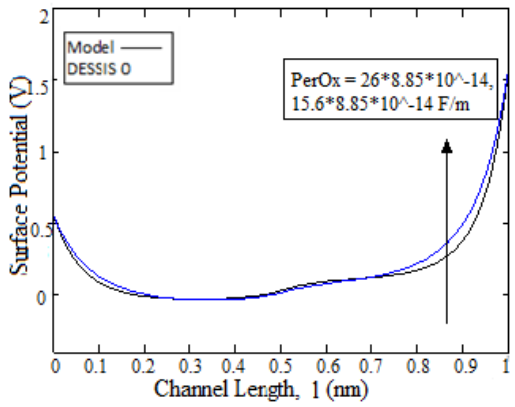

Fig. 9. Plot of surface potential v/s channel length for hfo2 and ta2o5 obtained by varying oxide permittivity using ta2o5 permittivity = 26*8.85*10-14 f/m, hfo2 permittivity = 15.6*8.85*10-14 f/m and keeping $\boldsymbol{v_{sb}}$= 0 V, $\boldsymbol{v_{gs}}$= 0 V, $\boldsymbol{v_{gb}}$= 0 V, w1 = 4.25 eV, w2 = 4.1 eV and $\boldsymbol{W_s}$= 4.68 eV constant.

From Figs. 6 and 7 it is seen that as the work function difference is increased the surface potential minima shifts downwards. Figs. 8 and 9 shows that as the permittivity of the dielectric material is increased the surface potential decreases at the two ends since the capacitances increase.

4 CONCLUSION

The paper presents a model for sub threshold surface potential and threshold voltage for an asymmetric Double halo Dual Material Gate (DHDMG) MOSFET. A vertical Gaussian doping profile in the channel is used here. Two gradual Gaussian doping profiles at the source and the drain ends are used to obtain the model. It is further reduced to a useful compact expression. The model also studies the effects of doping profile parameters and device parameters on the threshold voltage of the DHDMG devices. The model results and the results obtained from the 2D-device simulator DESSIS for channel lengths above 30 nm are in good agreement. It is also observed that when the gate oxide thickness reduces, the device dimension is reduced. High-k materials are used instead of silicon dioxide, namely Hafnium oxide (HfO2), Tantalum pentoxide (Ta2O5) to overcome this. The various device parameters and bias voltages are varied to validate the models.

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